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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	10/516,583
Filing Date	March 24, 2005
First Named Inventor	Charles Eugene Stroud
Art Unit	2863
Examiner Name	Demetrius R. Pretlow
Attorney Docket Number	46872-308797

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
DP	1.	US- 5,991,907	11-23-1999	Stroud et al.	
	2.	US- 6,108,808	08-22-2000	Abramovici et al.	
	3.	US- 6,256,758	07-03-2001	Abramovici et al.	
	4.	US- 6,530,049	03-04-2003	Abramovici et al..	
	5.	US- 6,574,761	06-03-2003	Abramovici et al.	
	6.	US- 6,874,108	03-29-2005	Abramovici et al.	
	7.	US- 6,973,608	12-06-2005	Abramovic et al.	
DP	8.	US- 6,996,020	02-07-2005	Yoshida	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	Demetrius Pretlow	Date Considered	6/4/07

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Sheet 2 of 3

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Filing Date	March 24, 2005
First Named Inventor	Charles Eugene Stroud
Art Unit	2863
Examiner Name	Demetrius R. Pretlow
Attorney Docket Number	46872-308797

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
DP	9..	ABRAMOVICI, M. et al., "Self-Test for FPGAS and CPLDs Requires No Overhead," Electronic Design, 1997, pp.121-128.	
	10.	ABRAMOVICI, M. et al., "Using Roving STARs for On-Line Testing and Diagnosis of FPGAs for Fault Tolerant Applications," Proc. IEEE International Test Conf., 1999, pp.973-982.	
	11.	ABRAMOVICI, M. and C. STROUD, "BIST-Based Diagnosis of FPGA Logic Blocks," Proc. IEEE International Test Conf., 1997, pp.539-547.	
	12.	ABRAMOVICI, M. et al., "Improving BIST-Based Diagnosis for Roving STARs," Proc. IEEE International On-Line Testing Symp., 2000, pp.31-39.	
	13.	ABRAMOVICI, M. and C. STROUD, "BIST-Based Test and Diagnosis of FPGA Logic Blocks," IEEE Transactions on Very Large Scale Integration Systems, 2001, 9(1):159-172.	
	14.	ABRAMOVICI, M. et al., "Roving STARs: An Integrated Approach to On-Line Testing, Diagnosis, and Fault Tolerance for FPGAs in Adaptive Computing Systems," Proc. NASA/DoD Evolvable Hardware Conf., 2001, pp.73-92.	
	15.	ABRAMOVICI, M. and C. STROUD, "BIST-Based Delay Fault Testing in FPGAs," Proc. IEEE International On-Line Testing Symp., 2002, pp.131-134.	
	16.	ABRAMOVICI, M. et al., "Using Embedded FPGAs for SoC Yield Enhancement," Proc. ACM/IEEE Design Automation Conf., 2002, pp.713-724.	
	17.	ABRAMOVICI, M. and C. STROUD, "BIST-Based Delay Fault Testing in Field Programmable Gate Arrays," J. Electronic Testing: Theory & Applications, 2003, 19(5):549-558.	
	18.	ABRAMOVICI, M. et al., "On-Line Built-In Self Test and Diagnosis of FPGA Logic Resources," IEEE Trans. On VLSI Systems, 2004, 12(12):1284-1294.	
	19.	CHEMLAR, E., "FPGA Interconnect Delay Fault Testing," Proc. Int'l Test Conf., 2003, pp.1239-1247.	
DP	20.	EMMERT, J. et al., "Dynamic Fault Tolerance in FPGAs via Partial Reconfiguration," Proc. IEEE International Symp. On Field-programmable Custom Computing Machines," 2000, pp.165-174.	

Examiner Signature	Demetrius Pretlow	Date Considered	6/4/07

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Filing Date	March 24, 2005
First Named Inventor	Charles Eugene Stroud
Art Unit	2863
Examiner Name	Demetrius R. Pretlow
Attorney Docket Number	46872-308797

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
DP	21.	EMMERT, J. et al., "Predicting Performance Penalty for Fault Tolerance in Roving Self-Testing Areas (STARs)," Proc. International Conf. On Field Programmable Logic, 2000, pp.545-554.	
	22.	EMMERT, J. et al., "On-Line Fault Tolerance for FPGA Interconnect with Roving STARs," Proc. IEEE International Symp. On Defect and Fault Tolerance in VLSI Systems, 2001, pp.445-454.	
	23.	STROUD, C. et al., "Built-in Self-Test of Logic Blocks in FPGAs," Proc. IEEE VLSI Test Symp., 1996, pp.387-392.	
	24.	STROUD, C. et al., "Evaluation of FPGA Resources for Built-In Self-Test of Programmable Logic Blocks," Proc. ACM International Symp. On Field Programmable Gate Arrays, 1996, pp.107-113.	
	25.	STROUD, C. et al., "Selecting Built-In Self-Test Configurations for Field Programmable Gate Arrays," Proc. IEEE Automatic Test Conf., 1996, pp.29-35.	
	26.	STROUD, C. et al., "Using ILA Testing for BIST in FPGAs," Proc. IEEE International Test Conf., 1996, pp.68-75.	
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	28.	STROUD, C. et al., "Built-In Self-Test of FPGA Interconnect," Proc. IEEE International Test Conf., 1998, pp.404-411.	
	29.	STROUD, C. et al., "On-Line BIST and Diagnosis of FPGA Interconnect Using Roving STARs," Proc. IEEE International On-Line Test Symp., 2001, pp.27-33.	
	30.	STROUD, C. et al., "BIST-Based Diagnosis of FPGA Interconnect," Proc. IEEE International Test Conf., 2002, pp.618-627.	
DP	31.	SMITH, J. et al., "An Automated BIST Architecture for Testing and Diagnosing FPGA Interconnect Faults," J. Electronic Testing: Theory & Applications, 2006, 22(4):239-253.	

Examiner Signature	Demetrius Pretlow	Date Considered	6/4/07

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